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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/575,561	05/21/2000	Paul F. Ferguson JR.	A0312/7408/MXS	1264

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EXAMINER

PHAN, TRONG Q

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 02/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/575,561

Applicant(s)

FERGUSON ET AL.

Examiner

TRONG PHAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Dec 31, 2001
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-52 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-52 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some\* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other:

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***Response to Arguments***

1. Applicant's arguments filed on 12/31/2001 have been fully considered to be persuasive. Therefore, the office action of 7/13/2001, paper # 6, has been withdrawn.

A new non-final Office action has been set forth as follow:

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-4 and 13-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fling et al., 4,591,832, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633.

Fling et al., 4,591,832, discloses in Fig. 1 a system comprising: signal preconditioner 12 for alternately providing digital samples of PCM binary samples in the luminance signal processing channel of a digital TV receiver (see lines 3436, column 2) to the common input of both DACs 16 and 18 connected in parallel (see lines 42-48, column 2); therefore, the first output analog signal 20 from the first DAC 16 is seen to be indicative of a sum of values of the input

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digital samples of PCM binary samples from signal preconditioner 12; and , alternately, the second output analog signal 22 from the second DAC 18 is seen to be indicative of a sum of values of the input digital samples of PCM binary samples from signal preconditioner 12 thereof; summing circuit 24 for producing the system common output signal at terminal 25.

What is not shown in Fling et al., 4,591,832, is the multi-bit digital signal as recited in claims 1-4 and 13-52.

Mehta et al., 4,205,203, discloses the teaching that digital samples of PCM binary samples are in the form of multi-bit digital signal (see the Summary of The Invention, lines 64-68, column 1 and lines 1-68, column 2).

In view of the above teaching of Mehta et al., 4,205,203, the input digital samples of PCM binary samples in the luminance signal processing channel of a digital TV receiver provided to the common input of both DACs 16 and 18 in Fig. 1 of Fling et al., 4,591,832, would have been obviously in the form of multi-bit digital signal as recited in claims 1-4 and 13-52.

What is not shown in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, is the signal conditioning stage comprising a switched capacitor filter as recited in claims 1-4 and 13-52.

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Lee et al., 6,130,633, discloses in Fig. 2A Prior Art the teaching of using switched capacitor filter 210 to be connected to the output of DAC 200.

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the switched capacitor filter 210 in Fig. 2A of Lee et al., 6,130,633, for connecting to the system common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, for the purpose of performing of lowpass filtering for removal of quantization noise in the system common output analog signal at common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203 (see lines 5-7, column 4 of Lee et al., 6,130,633).

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 5-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Myers, 5,798,724.

Myers, 5,798,724, discloses in Fig. 1 Prior Art a system comprising:

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finite impulse response (FIR) filter 12 for generating a sequence of N Bits digital words at an interpolation rate (see lines 14-18, column 1);

N BIT DAC 14;

reconstruct filter 16 which can be a switched capacitor filter (see lines 25-49, column 1);

as shown in Fig. 2, N BIT DAC 14 in Fig. 1 Prior Art can be implemented by the interpolating digital to analog converter 20 which includes: a first conversion stage 22 receiving an N bit data signal at an input rate (see lines 56-60, column 2) and a second conversion stage 26 in combination with interpolation stage 30 for providing an output analog signal 32 at an interpolation rate which is a multiple of the input rate (see lines 64-67, column 2).

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

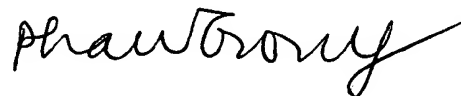
Kato et al., 4,580,126, Weigan et al., 4,430,642, Inami, 5,243,346, Law et al., 4,616,212, Lyden et al., 6,137,430, Noro, 5,818,372, and Anagnos, 6,150,970.

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7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (703) 308-4870 and email address is [trong.phan@uspto.gov](mailto:trong.phan@uspto.gov)

A handwritten signature in black ink, appearing to read 'Phan Trong', with a long horizontal stroke extending to the right.

**TRONG PHAN  
PRIMARY EXAMINER**

February 1, 2002